Sub B1

1. ~~(Amended) A shift register~~, comprising:

flip flops of a plurality of steps that output a signal in synchronization with a clock signal, and

a level shifter for increasing a voltage of a clock signal smaller in an amplitude than a driving voltage of said flip flop and for applying the clock signal to each of said flip flops, said shift register transmitting an input pulse in synchronization with the clock signal,

wherein said flip flops are divided into a plurality of blocks, each including at least one of said flip flops,

said level shifter is provided for each of said blocks, and

among a plurality of said level shifters, at least one of said level shifters, which correspond to blocks requiring no clock signal input for transmitting the input pulse, is ~~suspended~~ at that point.

Sub B2

20. ~~(Amended) A shift register, in which a plurality of flip flops are connected, for~~ transmitting an input pulse in synchronization with a ~~clock signal~~ and for outputting a signal,

said shift register comprising a plurality of level shifters for level-shifting the clock signal, said level shifter being provided for every predetermined number of said flip flops.

Please add the following new claims:

22. (New) The shift register as set forth in claim 1, wherein the level shifter operates in response to the input pulse that has been successively transmitted.

23. (New) The shift register as set forth in claim 22, further comprising:

a judging section, which identifies, based on the input pulse and an output signal, a level shifter which corresponds to blocks requiring no clock signal input, so as to control the input pulse into the level shifter.